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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,502	10/03/2003	Yi-Tsung Cheng	HTCP0013USA	2501

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EXAMINER	
BECK, ALEXANDER S	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
03/21/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/605,502	CHENG, YI-TSUNG	
	Examiner	Art Unit	
	ALEXANDER S. BECK	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-15,17,19,21,23,25 and 26* is/are allowed.

6)☒ Claim(s) *1-6,16,18,20,22 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on Dec. 12, 2007, has been entered. Claims 1-26 are currently pending and an Office action on the merits follows.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 16, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over an English translation of JP Patent No. 62-251917 to Nakazawa et al. ("Nakazawa") in view of U.S. Patent No. 4,414,538 to Schnizlein ("Schnizlein").

As to claim 1, Nakazawa discloses a keyboard comprising a key module (10) comprising at least one key cell with an output end being selectively connected to one of a first voltage and a second voltage (Nakazawa, pp. 5-6 and 8). A detect circuit (20) is electrically connected to the output end of the key cell for generating a control signal whenever the output end of the key cell becomes connected to the other of the second voltage and the first voltage (Nakazawa, pp. 5-6 and 8). A processor (21) is electrically connected to the detect circuit (Nakazawa, pp. 6-8). Furthermore, the control signal is generated such that the processor (21) does not poll for a status of the key cells during a

time period between any key cell being connected to the first voltage (e.g., key up) and then connected to the second voltage (e.g., key down) (Nakazawa, pp. 5-6 and 8).

Nakazawa does not disclose expressly a parallel-to-serial register electrically connected to the output end of the key module; and the processor electrically connected to the parallel-to-serial register and the detect circuit controlling the parallel-to-serial register according to the control signal. However, the use of a parallel-to-serial register in keyboard applications is old and well known in the art for converting parallel output data into serial output data for transmission to additional processing equipment. For example, Schnizlein discloses a keyboard comprising a parallel-to-serial register (64) electrically connected to the output end of a key module, wherein the parallel-to-serial register is operative in response to a signal representative of a depressed key cell (Schnizlein, col. 4 ll. 2-19).

All of the component parts are known in Nakazawa and Schnizlein. The only difference is the combination of the "old elements" into a single keyboard. Thus, it would have been obvious to a person of ordinary skill in the art to implement the parallel-to-serial register taught by Schnizlein into the keyboard of Nakazawa, since a parallel-to-serial register could be used in combination with a standard keyboard to achieve the predictable result of converting parallel output data into serial output data for transmission to additional processing equipment. As such, the modified embodiment comprising the processor of Nakazawa electrically connected to the parallel-to-serial register, and the detect circuit of Nakazawa controlling the parallel-to-serial register according to the control signal, wherein the control signal is generated whenever the output end of the key cell becomes connected to the other of the second voltage and the first voltage.

As to claim 16, all of the claimed limitations have already been discussed and met by Nakazawa and Schnizlein, as detailed in the above paragraphs with respect to claim 1.

For example, Nakazawa as modified by Schnizlein teaches/suggests a parallel-to-serial register for inputting data from the output end when the key cell is pressed or released; and a processor for controlling the parallel-to-serial register and reading the input data therein only upon reception of the control signal (Nakazawa, pp. 6-8) (Schnizlein, col. 4 ll. 2-19).

As to claims 18 and 20, Nakazawa as modified by Schnizlein teaches/suggest a plurality of key cells each having an output end connected to one of the first voltage and the second voltage; and the parallel-to-serial register electrically connected to the output end of each of the key cells in the key module for reading a parallel input being the voltage at the output end of all the key cells and converting the parallel input into a serial representation for output to the processor (Nakazawa, pp. 6-8) (Schnizlein, col. 4 ll. 2-19).

4. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa and Schnizlein as applied to claims 1, 16, 18 and 20 above, and further in view of U.S. Patent No. 4,027,306 to Hackmeister ("Hackmeister").

As to claims 2 and 3, note the above discussion of Nakazawa and Schnizlein. Neither Nakazawa nor Schnizlein disclose expressly wherein the detect circuit comprises at least one capacitor corresponding to and electrically connected to the at least one key cell within the key module and an amplifying circuit electrically connected to the capacitor for amplifying the voltage in the capacitor. However, the use of a capacitive element for storing a voltage and an amplifier to amplify the voltage is old and well known in the art during the pre-processing steps of an electronic device for an improvement in processing. Hackmeister discloses a touch-responsive circuit and data input terminal comprising: a key module (11) comprising at least one key cell (13') and a

detect circuit (12) comprising at least one capacitor (26) corresponding to each key cell within the key module and an amplifying circuit (28) for amplifying the voltage in the capacitor (Hackmeister, col. 3, l. 64 – col. 4, l. 21).

All of the component parts are known in Nakazawa, Schnizlein and Hackmeister. The only difference is the combination of the "old elements" into a single keyboard. Thus, it would have been obvious to a person of ordinary skill in the art to implement the at least one capacitor and amplifying circuit taught by Hackmeister into the keyboard taught by Nakazawa and Schnizlein, since a capacitor and amplifying circuit could be used in combination with a standard keyboard to achieve the predictable result of conducting a voltage indicative of a depression of the key cell followed by the sufficient amplification of the conducted voltage by an amplifier to a level applicable for use during processing.

5. Claims 4-6, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa, Schnizlein and Hackmeister as applied to claims 1-3, 16, 18 and 20 above, and further in view of U.S. Patent No. 6,265,993 to Johnson ("Johnson").

As to claims 4 and 5, note the above discussion of Nakazawa, Schnizlein and Hackmeister. Nakazawa as modified by Schnizlein and Hackmeister teaches/suggests the comparator electrically connected to the amplifying circuit, for comparing whether the voltage of the output end of the amplifying circuit is in a predetermined range and generating the control signal accordingly (Nakazawa, pp. 5-6, 8). Neither Nakazawa, Schnizlein nor Hackmeister disclose expressly a positive comparator and a negative comparator for generating the control signal when the voltage output from the output end of the amplifying circuit exceeds a positive reference voltage, and a negative comparator for generating the control signal when the voltage output from the output end of the amplifying circuit is lower than a negative reference voltage. Johnson discloses a

keyboard comprising a pair of detection means (72/74) for allowing the keyboard to separately identify positive and negative key group input signals and thereby distinguish key presses from key releases (Johnson, col. 6, ll. 19-42; see also col. 7, ll. 56-65).

All of the component parts are known in Nakazawa, Schnizlein and Hackmeister. The only difference is the combination of the "old elements" into a single keyboard. Thus, it would have been obvious to a person of ordinary skill in the art to implement the positive comparator and the negative comparator taught by Hackmeister into the keyboard taught of Nakazawa, Schnizlein and Hackmeister, since a positive comparator and a negative comparator could be used in combination with a standard keyboard to achieve the predictable result of allowing the keyboard to separately identify positive and negative key group input signals and thereby distinguish key presses from key releases.

As to claims 6, note the above discussion of Nakazawa, Schnizlein, Hackmeister and Johnson. Neither Nakazawa, Schnizlein, Hackmeister nor Johnson disclose expressly wherein the detect circuit comprises an OR gate for performing the step of determining whether a control signal is to be output. However, the examiner takes Official Notice that the use of an OR gate to perform a simple Boolean expression such as determining whether any of a plurality of inputs are high (e.g., determining which keys are within a predetermined range so as to output a control signal) is old and well known in the art.

Thus, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to further modify the teachings of Nakazawa, Schnizlein, Hackmeister and Johnson such that the step of determining whether a control signal is to be output was performed by an OR gate. The suggestion/motivation for doing so would have been because OR gates are very common in the art, readily available, and cheap to manufacture. Moreover, an OR gate can be used in combination with a standard keyboard receiving a plurality of inputs for the predictable results of determining whether there are any keys within a predetermined range so as to output a control signal.

As to claim 24, note the above discussion with respect to claims 4 and 5. For similar reasons, Nakazawa as modified by Schnizlein, Hackmeister and Johnson teaches/suggests wherein the detect circuit is further for asserting the control signal only while detecting the transient voltage being greater than a reference voltage, the transient voltage corresponding to a change in voltage at the output end of the key cell and being a voltage spike that occurs at the moment the key cell is pressed and at the moment the key cell is released (Nakazawa, pp. 6-8) (Johnson, col. 6, ll. 19-42; see also col. 7, ll. 56-65).

6. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa and Schnizlein as applied to claims 1, 16, 18 and 20 above, and further in view of Johnson.

As to claim 22, note the above discussion with respect to Nakazawa and Schnizlein. Neither Nakazawa nor Schnizlein disclose expressly wherein the detect circuit is further asserted for asserting the control signal only while detecting a transient voltage being greater than a reference voltage, the transient voltage corresponding to a change in voltage at the output end of the key cell and being a voltage spike that occurs at the moment the output end of the key cell becomes connected to the other of the second and the first voltage, as claimed. Johnson discloses a method of detecting a key press, similar to that of Nakazawa, wherein the key press corresponds to a transient voltage being greater than a reference voltage, the transient voltage corresponding to a change in voltage at the output end of the key cell and being a voltage spike that occurs at the moment the output end of the key cell becomes connected to the other of the second and the first voltage (Johnson, col. 6, ll. 19-42; see also col. 7, ll. 56-65). Because both Nakazawa/Schnizlein and Johnson teach methods of detecting a key press in a keyboard,

it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable result of detecting a valid key press.

Allowable Subject Matter

7. Claims 7-15, 17, 19, 21, 23, 25 and 26 are allowed.

8. The following is an examiner's statement of reasons for allowance:

As to claims 7 and 17, the prior art of record fails to teach or suggest a keyboard comprising: a key module; a detect circuit for generated a control signal when a key is pressed and released; and a processor for controlling the parallel-to-serial register only upon reception of the control signal without polling for a status of the key cells during a time period between any key cell being pressed and then released, as claimed.

As to claim 26, the prior art of record fails to teach or suggest a keyboard, comprising: a plurality of keys; a plurality of capacitors; an amplifier, a first comparator; a second comparator; a logical OR gate outputting a control signal to indicate that one of the key cells has been pressed and to indicate that one of the key cells has been released; and a parallel-to-serial register coupled to the processor, without the processor polling for a status of the key cells during a time period between any key cell being pressed and then released, as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

9. Applicant's arguments filed Dec. 17, 2007, with respect to claims 1-6, 16, 18, 20, 22 and 24 have been fully considered but they are not persuasive.

Applicant argues there is a lack of motivation to combine the teachings of Schnizlein and Nakazawa (Remarks, pp. 9-10). Examiner respectfully disagrees and submits that the combination of prior art elements according to known methods to yield predictable results, as detailed in the rejection, is a rationale that supports a conclusion of obviousness (MPEP § 2141(III)).

Applicant argues that Nakazawa fails to teach or suggest "without polling for a status of the key cells during a time period between any key cell being connected to the first voltage and then connected to the second voltage", as claimed (Remarks, pp. 10-12). Examiner respectfully disagrees and submits that Nakazawa does teach this newly amended limitation if the "first voltage" is interpreted to be the key-up voltage and the "second voltage" is interpreted as the key-down voltage (Nakazawa, pp. 5-6 and 8).

Applicant argues that it would not have been obvious to modify the teachings of Nakazawa and Schnizlein by Hackmeister because of the unnecessary components it would introduce (Remarks, pp. 12-13). Examiner respectfully disagrees and submits that the combination of prior art elements according to known methods to yield predictable results, as detailed in the rejection, is a rationale that supports a conclusion of obviousness (MPEP § 2141(III)).

10. Applicant's arguments filed Dec. 17, 2007, with respect to claims 7-15, 17, 19, 21, 23, 25 and 26 have been fully considered and are persuasive. The rejections of claims 7-15, 17, 19, 21, 23, 25 and 26 have been withdrawn in light of the new amendments to the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALEXANDER S. BECK whose telephone number is (571)272-7765. The examiner can normally be reached on M-F, 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

asb
Mar. 10, 2008